REMARKS

Claims 28-35, 38-54, and 56-73 are pending and presented for reconsideration.

Rejection of claims under 35 U.S.C. § 103

Claims 28-35, 38-40, 43, and 45 are rejected under 35 U.S.C. § 103(a) as being unpatentable over K. Ismail, "Si/SiGe High-Speed Field Effect Transistors," *IEEE IEDM Tech. Dig.*, pp. 509-512, 1995 ("Ismail") in view of Chang et al., "Selective Etching of SiGe on SiGe/Si Heterostructures," *J. Electrochem Soc.*, Vol. 138, No. 1, pp. 202-204, January 1991 ("Chang") and P.-E. Hellberg, et al., "Oxidation of silicon-germanium alloys. I. An experimental study," *J. Appl. Phys.*, Vol. 82, No. 11, pp. 5773-5778, December 1997 ("Hellberg"). Ismail appears to disclose designs for SiGe-based modulation-doped field-effect transistors and metal-oxide-semiconductor field-effect transistors. *See* Ismail, Figured 7, 9, and related text. Chang appears to disclose methods for selectively etching SiGe over Si. *See* Chang, abstract. Hellberg appears to disclose a study involving the oxidation of polycrystalline SiGe samples having different Ge contents. *See* Hellberg, abstract. The Examiner relies on Ismail to teach all of the limitations of independent claim 28, except for 1) selectively removing a SiGe layer to expose a strained semiconductor layer, and 2) selective removal comprising thermal oxidation performed at or below a temperature of approximately 850 °C. The Examiner relies on Chang to supply the first feature, noting that Chang discloses only the chemical removal of SiGe. The Examiner relies on Hellberg to supply the second feature, stating that it would have been obvious to one of skill in the art to use thermal oxidation in the process of Ismail and Chang "for its known benefit of oxidizing SiGe surfaces as disclosed by Hellberg."

While Hellberg does disclose the fact that SiGe may be oxidized, the Examiner does not explain the basis for his contention that this is a "known benefit" justifying an obviousness rejection. In fact, one of skill in the art would not combine the oxidation process of Hellberg with Ismail and Chang, because Hellberg's process is more time-consuming than Chang's chemical etching and results in deleterious Ge interdiffusion and Ge contamination. In particular, Hellberg discloses that his oxidation process results in oxide thicknesses of approximately 75 to approximately 230 nm after oxidation times of 200 minutes, i.e., removal of approximately 37 to approximately 115 nm of underlying semiconductor material after 200

minutes. *See* Hellberg, Fig. 3. In contrast, Chang's method results in the removal of well over 250 nm of SiGe in only 2 minutes. *See* Chang, Fig. 5. One of skill in the art, wishing to remove SiGe, would clearly prefer the faster method of Chang, particularly since Hellberg's method also involves temperatures vastly higher than Chang's temperatures. Further, Hellberg makes patently clear the fact that his oxidation process results in the interdiffusion of Si and Ge and a "pile-up" of Ge beneath the forming oxide, a phenomenon which would "smear" the clearly defined layers of Ismail. *See* Hellberg, p. 5774, right column, first full paragraph, and p. 5777, left column, second full paragraph. Such a phenomenon would render the right-hand device of Ismail's Fig. 7 inoperable for its intended purpose, as it depends on a channel of pure Si to achieve high electron mobility. *See* Ismail, Fig. 7 and p. 509, section entitled Material Properties. Indeed, Hellberg's disclosure of Ge interdiffusion implies that his method would be incapable of selectively stopping on a Si layer, as Ismail's structure demands; Hellberg himself avoids this problem by oxidizing only polycrystalline SiGe films formed directly on SiO_2 layers. *See* Hellberg, Fig. 1, inset.

Applicants submit that, for at least these reasons, independent claim 28 and claims dependent therefrom, are patentable over the cited prior art.

Regarding dependent claim 43, the Examiner states that it would have been obvious to one of skill in the art to "use the MODFET and MOSFET structures on the same substrate, for their respective benefits as disclosed by Ismail." However, the Examiner again ignores the fact that Ismail himself teaches against the formation of a MOSFET on his Fig. 7 structure (which includes the "removed" SiGe layer portion required by dependent claim 43). As emphasized in previous Responses, Ismail only teaches the formation of MOSFETs on his planar structure of Fig. 9. Moreover, Ismail also discloses that the choice of MOSFET over MODFET comes at a cost of performance: The MODFETs in Ismail's Fig. 7 have transconductances higher than those of his MOSFETs. *See* Ismail, p. 510, right column, bottom paragraph, and p. 511, right column, first paragraph. One of skill in the art, having formed a structure similar to that of Ismail's Fig. 7 (as the instant claims require), would not then fabricate Ismail's inferior device upon it, particularly when the Fig. 7 structure is designed only for MODFETs. Applicants submit that, for at least this additional reason, dependent claim 43 is patentable over the cited art.

Regarding dependent claim 45, none of the cited art discloses forming a surface channel device and a buried channel device, both channels of which are disposed in a single strained semiconductor layer. While Ismail does disclose a surface channel device and a buried channel device in Fig. 7, these devices manifestly have channels in different layers of Ismail's structure. Ismail discloses that, in his structure, "electrons would flow through a strained Si layer, and the holes flow through a strained SiGe layer." *See* Ismail, p. 510, right column, bottom paragraph, and Fig. 7. Applicants submit that, for at least this additional reason, dependent claim 45 is patentable over the cited art.

Claims 41 and 43 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ismail in view of Chang and Hellberg, and further in view of U.S. Patent No. 6,044,255 to Suematsu et al. ("Suematsu") or U.S. Patent No. 6,191,432 to Sugiyama et al. ("Sugiyama"). The Examiner concedes that Ismail teaches that his Fig. 7 structure applies only to MODFETs (rather than the MOSFETs recited in these claims), but utilizes Suematsu and/or Sugiyama to disclose "the equivalence of MODFETs and MOSFETs in certain cases in integrated circuits."

While Suematsu and/or Sugiyama may stand for the proposition that, in certain circuits, a practitioner may choose between MOSFETs and MODFETs, these references do nothing to counter the fact that Ismail teaches against using MOSFETs in his Fig. 7 structure (i.e., a structure having a portion in which a SiGe layer may have been removed). Suematsu appears to disclose various radio-frequency circuits, at least one of which can include a silicon MOSFET or a "FET having another structure, for example, … [a] MODFET … to obtain a similar effect." *See* Suematsu, column 9, lines 35-38. Suematsu is utterly silent as to the physical layer structure required for the fabrication of MOSFETs or MODFETs, stating only that FETs "may be made of silicon or a compound semiconductor, such as SiGe, GaAs, or InP." *See* Suematsu, column 5, lines 50-52. Similarly, Sugiyama merely discloses in his background section that, when various layers are strained, either MOSFETs or MODFETs with certain characteristics may be fabricated. *See* Sugiyama, column 1, lines 38-62. Sugiyama is also utterly silent regarding physical layer structures suitable for MOSFETs or MODFETs; indeed, MODFETs are not even mentioned again in his entire patent. Thus, while MOSFETs and MODFETs may be

interchangeable for some circuit applications, they are not interchangeable in Ismail's circuit, as Ismail himself clearly teaches. Certainly nothing in Suematsu or Sugiyama counters Ismail's express teaching that MODFETs may be utilized with his Fig. 7 structure and MOSFETs may be utilized with his planar Fig. 9 structure. Suematsu and Sugiyama are simply irrelevant to, and do not nullify, the distinction drawn by Ismail. Applicants submit that, for at least this additional reason, dependent claims 41 and 43 are patentable over the cited art.

Claims 42 and 44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ismail in view of Chang, Hellberg, and Suematsu or Sugiyama, and further in view of U.S. Patent No. 6,271,094 to Boyd et al. ("Boyd"). Applicants submit that these claims are allowable for at least the reasons that independent claim 28 and dependent claims 41 and 43, from which they depend, are allowable.

Claims 46-54 and 56-73 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ismail in view of Chang and Suematsu or Sugiyama, and further in view of Boyd. The Examiner relies on Ismail to supply most of the elements of independent claims 46, 56, 58, 60, and 67, relying on Suematsu or Sugiyama to supply "the equivalence of MODFETs and MOSFETs in certain cases in integrated circuits" and Boyd to supply the use of a high-k dielectric in a MOSFET.

However, as described above in relation to dependent claims 41 and 43, none of the cited art, particularly Suematsu and Sugiyama, nullifies Ismail's express teaching that Ismail's Fig. 7 structure is incompatible with MOSFETs (with a high-k or other gate dielectric). Nor does any cited reference counter Ismail's statements that his planar Fig. 9 structure is the correct platform for MOSFETs, and even then, his MOSFETs have inferior electrical performance. Independent claims 46, 56, 58, 60, and 67 require the selective removal of a SiGe layer, followed by the fabrication of a MOSFET – steps Ismail teaches are incompatible, and none of the cited art teaches otherwise.

Moreover, with respect to independent claim 60, Ismail does not teach or suggest forming p-type-doped source and drain regions in any type of device fabricated in an exposed strained semiconductor layer after selective removal of a SiGe layer. Rather, Ismail teaches that, to form

a device with p-type-doped source and drain regions (e.g., a P-MODFET), the SiGe layer partially missing in Fig. 7 is required – it is this layer that functions as the channel of his P-MODFET device. *See* Ismail, Fig. 7 and p. 510, right column, bottom paragraph. One of skill in the art could not simply selectively remove this layer and then fabricate a device having p-type-doped source and drain regions, as the SiGe channel layer, from which the device derives its enhanced performance, would be missing.

Applicants submit that, for at least these reasons, independent claims 46, 56, 58, 60, and 67, and claims dependent therefrom, are patentable over the cited prior art.

CONCLUSION

In light of the foregoing, Applicants respectfully submit that all claims are now in condition for allowance.

Applicants believe that no additional fees are necessitated by the present paper. However, in the event that any additional fees are due, the Commissioner is hereby authorized to charge any such fees to Deposit Account No. 07-1700.

If the Examiner believes that a telephone conversation with Applicants' agent would expedite allowance of this application, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,

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Reg. No. 58,533

Electronic Signature: /Matthew T. Currie/
Matthew T. Currie
Agent for the Applicants
Goodwin | Procter LLP
Exchange Place
Boston, Massachusetts 02109

Tel. No.: (617) 570-1198
Fax No.: (617) 523-1231